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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,264	11/17/2003	Nathan R. Brown	2269-4375.3US (99-1029.03	5086

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TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
MACARTHUR, SYLVIA	

ART UNIT	PAPER NUMBER
1763	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,264	BROWN, NATHAN R.	
	Examiner	Art Unit	
	Sylvia R. MacArthur	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/31/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/6/2007 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection. Amended claim 1 was broadened to only require a method of polishing a semiconductor comprising the steps of polishing the semiconductor and analyzing the topography of that semiconductor after the polishing step. The prior art of Sahota et al (US 5,665, 199) teaches this in Fig.4 step 56 and 58 a-c, the prior art of Ritzdorf et al (US 2003/0020928) teaches a CMP processing unit with a post polishing metrology step see the abstract and Fig.c1, the prior art of Williams (US 6,594,542) teaches the step of CMP operation step 110 and measuring the finished wafer thickness after CMP see step 150, see Fig.1, the prior art of Patel et al (US 6,623,333) teaches a method of controlling a wafer polishing process (CMP) wherein step 16 is a polishing step and step 14 features post thickness metrology, see Fig.1, Campbell et al (US 6,454,899) teaches a polishing step 160/740 with a step of measuring the thickness step 170/750, see Figs. 1 and 7, Shanmugasundram et al (US 7,160,739) teaches feedback control of CMP wherein polishing processing parameters (such as pressure gradients)

are updated basis the feedback control using thickness measurements (metrology) as the basis of measurement, see abstract, Fig. 4, and col. 6 lines 45-52. Pasadyn et al (US 6,442,496) teaches using metrology as the basis of process control see Fig.1 in col. 8 lines 7-15 CMP is discussed as a processed in which the thickness of the wafer is monitored. New claim 15, recites the force gradients created in the process where different amounts of pressure are applied to the backside of the semiconductor. The prior art of Korovin (US 6, 544, 103) teaches a pressure profile created by zones with a wafer carrier, see abstract and Fig. 1. **Note this is a different prior art to Korovin et al than in the previous rejection. Wang et al (US 6,857,947) teaches an advanced CMP system wherein a plurality of pressure zones are configured to selectively apply pressure to the polishing member see the abstract and Figs. 9a and 9b. Wu (US 6,270,397) teaches a CMP device with a pressure mechanism where different pressures along the semiconductor are created in response to different polishing rates see the abstract.

The arguments filed 2/16/2007 found on pages 8-11 and the examiner's reply (seen in italics) can be summarized below:

A) Measuring a film thickness over a measureable topographic features is not analyzing the topography of an active surface. *It is the examiner's position that the concept of topography amounts to the physical differences in an object in this case a wafer. In the case of the prior art of Sahota, Sahota quantifies the physical differences along the wafer surface by measuring the thickness at various locations see col.5 lines 6-24.It is the examiner's position that measuring the film thickness in different locations along the wafer is a way to quantify the topography.*

B) Neither Saka et al nor Sahota et al teach the step of analyzing the topography of an active surface. *The examiner denotes topography as noting the physical features of an object such as the varying heights along the surface of the wafer. It is the examiner's position that the prior art of Sahota et al analyzes the topography by noting the differences in film coating thickness along the wafer see col.2 lines 5-39, col. 4 lines 65 and 66. The prior art of Sato is used to teach performing a CMP process using non-uniform pressure profiles (pressure gradients) on the backside of a wafer, see col. 7 lines 14-40. The prior art of Saka et al was combined with the teachings of the prior art of Sahota et al which teaches the step of polishing a first wafer, analyzing its thickness (providing a topography/metrology step) see steps 58a-c after the polishing step and polishing additional wafers see step 66 in Fig.4.*

C) The combination of Nagahara in view of Sahota fails to teach a pressure gradient. *The examiner disagrees with applicant's assertion that Nagahara et al fails to teach pressure gradients as the abstract clearly states that the planarizing of the wafer is provided by applying non-uniform pressure distributions across the backside of the wafer. The prior art of Nagahara is used to teach performing a CMP process using non-uniform pressure profiles (pressure gradients) on the backside of a wafer, see the abstract and cols. 4-8 as support. The prior art of Nagahara et al was combined with the teachings of the prior art of Sahota et al which teaches the step of polishing a first wafer, analyzing its thickness (providing a topography/metrology step) see steps 58a-c after the polishing step and polishing additional wafers see step 66 in Fig.4.*

D) There is no motivation to combine the teachings of the prior art of Korovin et a al (US 6,90,905) in view of Sahota et al.

Upon further review, the examiner notes that though Korovin teaches a method of selecting a CMP carrier with adjustable pressure zones that correspond to the number and location of the bulges and troughs on the wafer, from this recitation in the abstract, the examiner deduces that the analysis of the topography (bulges and troughs on the wafer) takes places prior to the polishing step. Newly amended claim 1 requires that such analysis take place after the polishing step. Thus the rejection of Korovin et al in view of Sahota et al is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Shanmugasundram et al (US 7,160,739).

Shanmugasundram et al teaches a feedback control of CMP by manipulating the removal rate profiles.

Regarding claims 1 and 3: The prior art of Shanmugasundram et al teaches a method comprising the step of polishing the wafer (semiconductor device structure) and analyzing the topography of the wafer after the polishing step, see the abstract. The topography of the wafer is quantified by determining the thickness profile of the wafer.

Regarding claims 15, 5,6, 8, 9, 13, and 14: A force gradient is generated including a plurality of immediate adjacent distinctly different amounts of pressure see col. 6 lines 48-50 and col. 7 lines 45- col. 8 line 4. A polishing recipe is determined from the thickness analysis to determine the optimal pressure zones see co. 9 and 10. Shanmugasundram et al features a feedback and feed forward control that can update the processing parameters such as pressure variations for subsequent wafers, see col. 10 lines 35-38.

Regarding claims 2, 7, 8, 11, and12: The type of polishing referred to in Shanmugasundram et al is CMP, see the title.

Regarding claims 4 and 10: See the title and step 500 wherein polishing rate is taken into account.

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Sahota et al (US 5,665,199).

Sahota et al teaches polishing a wafer (semiconductor device) and measuring the thickness (quantifies the topography/metrology step) of the wafer in different locations along the wafer, this in Fig.4 step 56 and 58 a-c, t.

6. Claims 1-3, 6-9, and 11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Korovin et al (US 6,544,103).

Regarding claim 1-3 and 15: Korovin teaches applying a pressure profile using an enhanced CMP carrier, see abstract. A wafer is polished and is post-CMP thickness profile is determined and used to devise the optimum geometry for a multizone carrier, see col. 3 lines 65. The carrier will create a particular pressure distribution profile on the back surface of a wafer

dependent on the number of zones and the pressure within each zone. The thickness profile is measuring using a metrology system see col. 3 liens 33-64.

Regarding claims 6-9 and 13: see col. 4 lines 9-15.

Regarding claims 11 and 12: The type of polishing is CMP see the title.

Regarding claim 14: The updated pressure profile address the simultaneously application of increased amounts of pressure, see col. 4 lines 55-67.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 6-8, and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saka et al (US 6,476,921) in view of Sahota et al (US 5,665,199).

The teachings of Sahota were discussed above.

Sahota et al fails to teach the specific polishing steps other than the polishing recipe is updated based on the topography see col. 17 and 18.

Saka et al teaches a method of polishing a semiconductor using different pressure zones, see abstract and Fig.4.

Re Claims 8and 9: The method of Saka et al teaches selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the

semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see col. 7 lines 1-40.

Re Claims 2, 7, 11, 12: The polishing discussed in Saka et al is CMP according to the title.

Re Claim 6, 13 and 14: The different amounts of pressure are provided by biasing independently movable pressurization structures, see col. 7 lines 1-40 and Fig. 4.

Re Claim 14: The polishing of Saka et al comprises forming a substantially planar surface on the semiconductor device structure, see abstract.

Saka et al fails to polishing a second semiconductor structure based on the applied pressure of the first.

Sahota et al teaches a methodology of developing product specific interlayer dielectric polish processes. Sahota et al illustrates in Fig. 4, the polishing of a first wafer and measuring the topography of that first wafer, then using the first data points to polish a subsequent wafer. Topography (surface profile measurements) is discussed in col. 17 lines 18-26 and col.15 lines 45-67.

The motivation to modify the teachings of Saka et al is to enhance the capabilities of the apparatus from the application of pressure to a specific wafer to wafers in an entire lot or batch. The combined teachings of Saka et al and Sahota et al will increase throughput and the uniformity of polishing with a lot of wafers. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to combine the teachings of Saka and Sahota et al to provide a CMP process with a processing model and parameters that are optimized via the topography of the wafers are quantified by the thickness measurement profiles.

The examiner denotes topography as noting the physical features of an object such as the varying heights along the surface of the wafer. It is the examiner's position that the prior art of Sahota et al analyzes the topography by noting the differences in film coating thickness along the wafer see col.2 lines 5-39, col. 4 lines 65 and 66. The prior art of Sato is used to teach performing a CMP process using non-uniform pressure profiles (pressure gradients) on the backside of a wafer, see col. 7 lines 14-40. The prior art of Sato was combined with the teachings of the prior art of Sahota et al which teaches the step of polishing a first wafer, analyzing its thickness (providing a topography/metrology step) see steps 58a-c after the polishing step and polishing additional wafers see step 66 in Fig.4.

9. Claims 2, 6-8, and 11-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagahara et al(US 6,531,397) in view of Sahota et al (US 5,665,199).

Nagahara et al teaches a method of CMP using wafer back pressure differentials, see title.

Re Claims 8 and 9: The method of Chen et al teaches selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see col. 5 and 6

Re Claim 6, 13, and 14: The different amounts of pressure are provided by biasing independently movable pressurization structures see abstract and cols. 5 and 6.

Re Claims 2,7, 11, 12:The polishing discussed in Nagahara et al is CMP according to the title.

Re Claim 14: The polishing of Nagahara et al comprises forming a substantially planar surface on the semiconductor device structure, see abstract.

Nagahara et al fails to polishing a second semiconductor structure based on the applied pressure of the first.

Sahota et al teaches a methodology of developing product specific interlayer dielectric polish processes. Sahota et al illustrates in Fig. 4, the polishing of a first wafer and measuring the topography of that first wafer, then using the first data points to polish a subsequent wafer. Topography (surface profile measurements) is discussed in col. 17 lines 18-26 and col.15 lines 45-67.

The motivation to modify the teachings of Nagahara et al is to enhance the capabilities of the apparatus from the application of pressure to a specific wafer to wafers in an entire lot or batch. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to combine the teachings of Nagahara et al and Sahota et al as the modification will increase throughput and the uniformity of polishing with a lot of wafers.

The prior art of Nagahara is used to teach performing a CMP process using non-uniform pressure profiles (pressure gradients) on the backside of a wafer, see the abstract and cols. 4-8 as support. The prior art of Nagahara et al was combined with the teachings of the prior art of Sahota et al which teaches the step of polishing a first wafer, analyzing its thickness (providing a topography/metrology step)see steps 58a-c after the polishing step and polishing additional wafers see step 66 in Fig.4.

10. Claims 4,5, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art of Korovin et al in view of Wu (US 6,270,397) or the prior art of Saka et al or Nagahara et al in view of Sahota et al as applied in paragraphs 8 and 9 respectively in further view of Wu (US 6,270,397).

The teachings of Wu et al and Saka et al or Nagahara et al in view of Sahato et al were discussed above. All fail to teach the consideration of rate of removal in their process control method.

Wu teaches a CMP device with a pressure mechanism wherein the different pressures exerted on the different locations along the wafer are determined basis the different polishing rates at the specific locations, see Figs. 2A and 2B and col. 3 lines 27-63.

The motivation to incorporate the teachings of Wu in the method of Korovin or Wu in the method of Saka et al or Nagahara et al in view of Sahota et al is that the method further enhances the polishing process by considering that the varied topography along the wafer surface will require different polishing rates. The greater the thickness at a specific location the more time required to polish that section and thus an increased rate is required so that that the entire wafer will be polished within a desired time interval. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to incorporate the teachings of Wu in the method of Korovin or Wu in the method of Saka et al or Nagahara et al in view of Sahota et al is that the method further enhance the polishing process.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sylvia R. MacArthur whose telephone number is 571-272-1438. The examiner can normally be reached on M-Th during the hours of 8 a.m. and 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sylvia R MacArthur
Primary Examiner
Art Unit 1763

May 14, 2007